WHAT IS CLAIMED IS:

1. A design method for changing layout results of a semiconductor integrated circuit, the method comprising the steps of:

detecting a branching point of a wire in the layout results including information regarding types of cells, information regarding arrangement of the cells, and information regarding wiring among the cells;

virtually inserting a load having a predetermined amount at a predetermined point on one of wires subsequent to the detected branching point;

calculating a delay amount of each route connecting cells via the branching point with the load being inserted and a delay amount thereof without the load being inserted;

determining, based on the delay amounts of each route, an insertion point at which a load-dividing buffer is to be inserted;

calculating a drive capability of a driving cell preceding the insertion point, on condition that the load-dividing buffer is to be inserted at the determined insertion point and based on timing constraints of each route;

deciding, based on the layout results, whether the load-dividing buffer is insertable at the insertion point; and

performing a process of changing the layout results based on the decision results, the process including a process of placing

the load-dividing buffer at the insertion point, a process of changing the driving cell to a cell having the calculated drive capability, and a process of changing wiring information in accordance with circuit changes.

2. The semiconductor integrated circuit design method according to claim 1, wherein

when a delay amount of a route determined under predetermined decision criteria as having tight timing constraints is changed by an amount larger than a predetermined amount with the load being virtually inserted at the predetermined point, the insertion point determining step determines the predetermined point as the insertion point at which the load-dividing buffer is to be inserted.

3. The semiconductor integrated circuit design method according to claim 2, wherein

of routes connecting cells via the branching point, the insertion point determining step determines a route having tightest timing constraints as having tight timing constraints.

4. The semiconductor integrated circuit design method according to claim 1, wherein

the load inserting step virtually inserts the load at the predetermined point on the wire subsequent to the detected

branching point when it is determined in accordance with predetermined criteria that the load is required.

5. The semiconductor integrated circuit design method according to claim 4, wherein

the load inserting step includes the steps of:

calculating a total load capacitance after the branching point;

calculating a total load capacitance of the driving cell; and

virtually inserting the load at the predetermined point on the wire subsequent to the branching point when a ratio of the total load capacitance after the branching point to the total load capacitance of the driving cell is larger than a predetermined value.

6. The semiconductor integrated circuit design method according to claim 4, wherein

the load inserting step includes the steps of:

calculating, for each of the wires subsequent to the branching point, a total load capacitance after one of the wires; and

virtually inserting the load at the predetermined point on the wire so that the total load capacitance after the wire is largest of all total load capacitances for the wires

subsequent to the branching point, in a case where the total load capacitances are unbalanced to a degree higher than a predetermined degree.

7. The semiconductor integrated circuit design method according to claim 4, wherein

the load inserting step includes the steps of:

calculating, for each of the wires subsequent to the branching point, a worst value of timing constraints of a route including one of the wires; and

virtually inserting the load at a predetermined point on a wire whose worst value of timing constraints indicates timing constraints tightest of all the calculated worst values of timing constraints, in a case where the worst values of timing constraints for the wires subsequent to the branching point are unbalanced to a degree higher than a predetermined degree.

8. The semiconductor integrated circuit design method according to claim 4, further comprising

prior to the route delay amount calculating step, a step of detecting, in the layout results, a deletable buffer which has no influence on a logic function of the circuit and is connected at an output terminal to the wire having the branching point, wherein

the route delay amount calculating step further calculates a delay amount of a route connecting a cell preceding

the deletable buffer and a cell immediately subsequent to the deletable buffer with the deletable buffer being virtually deleted, and

the layout results changing step further performs a process of deleting the deletable buffer from the layout results.

9. A method of obtaining delay information regarding delays occurring when load division is performed based on layout results of a semiconductor integrated circuit, the method comprising the steps of:

detecting a branching point on a wire in the layout results including information types of cells, information regarding arrangement of the cells, and information regarding wiring among the cells;

virtually inserting a load having a predetermined amount at a predetermined point on a wire subsequent to the detected branching point; and

calculating a delay amount of a route connecting cells via the branching point with the load being inserted and a delay amount thereof without the load being inserted.

10. The delay information calculating method for the semiconductor integrated circuit according to claim 9, wherein

the load inserting step virtually inserts the load at the predetermined point on the wire subsequent to the detected

branching point when it is determined in accordance with predetermined criteria that the load is required.

11. The delay information calculating method for the semiconductor integrated circuit according to claim 9, further comprising

prior to the route delay amount calculating step, a step of detecting, in the layout results, a deletable buffer which has no influence on a logic function of the circuit and is connected at an output terminal to the wire having the branching point, wherein

the route delay amount calculating step further calculates a delay amount of a route connecting a cell preceding the deletable buffer and a cell immediately subsequent to the deletable buffer with the deletable buffer being virtually deleted.